A SI BJT RF DUAL BAND RECEIVER IC FOR DAB

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ABSTRACT

A low cost 1.5 GHz and 200 MHz dual channel broadband receiver IC for Digital Audio Broadcast (DAB) is described. The SSOP-28 packaged Si bipolar device provides 28 dB of conversion gain, 4 dB NF and 50 dB IM3 suppression to a common 920 MHz IF. Two novel 30 dB variable gain, 2.4 dB NF, low noise amplifiers are integrated with doubly balanced mixers, VCO, dual modulus prescaler, AGC and power management circuitry. With a companion IF IC, filters, and 20 MHz Frequency Synthesizer, it forms a complete DAB receiver for large dynamic range signals between –97 and -5 dBm.

INTRODUCTION

As part of a two chip set which provides a complete RF receiver for terrestrial or satellite broadcast DAB , the IC (RFIC) presented in this paper, converts L-Band (1452 – 1492 MHz) signals and Band III (170 – 240 MHz) signals between –97 and -5 dBm to a common 920 MHz first IF. A 10 MHz bandwidth SAW filter precedes the second IC (IFIC) [1] that converts the signals to a 30 MHz second IF where the 1.536 MHz bandwidth DAB signal is selected by a second SAW filter and amplified for the A/D. The large 40 MHz and 70 MHz receive bandwidths of L-Band and Band III channels respectively require the RFIC to receive all DAB signals and strong neighboring interference while maintaining high linearity. Novel, AGC leveled, variable gain LNA designs are developed, enabling this alternative DAB receiver architecture [2] to cope with high interference levels without requiring a tunable preselect filter which would increase receiver cost and complexity. Together the two ICs [3] provide a low cost solution for manufacturers seeking to add L-Band and Band III DAB functionality to a "dash-board compatible" consumer electronics car radio.

CHIP TOPOLOGY

Figure 1 shows the block diagram of the chip. The IC integrates two variable gain LNAs, two mixers, a VCO and a dual modulus divide by 64/65 prescaler. The LNAs have 2.4 dB NF, 20 dB gain, variable gain ranges of more than 30 dB and more than 40 dB IM3 suppression. Their leveled output of about -20 dBm is image filtered on-chip in the L-Band channel and off-chip in Band III before driving low current, high linearity modified Gilbert cell mixers and IF buffer amplifiers to produce 26 dB L Band and 28 dB Band III total conversion gain. A low phase noise 1064 - 1160 MHz tunable local oscillator (LO) is generated by phase locking the on-chip VCO using an external low cost, low frequency, programmable frequency synthesizer, such as the CMOS Plessey NJ88C33, whose inputs are the 16.4 - 18.2 MHz prescaler output and the DAB system reference clock. Also integrated are 920 MHz IF buffer amplifiers, LO buffer amplifiers and a divide by 2 which generates a 532 - 572 MHz LO for the L-Band mixer. Completing the integration are band switch, power management, a unique AGC pause control and all AGC control circuitry except for the integrating capacitor.

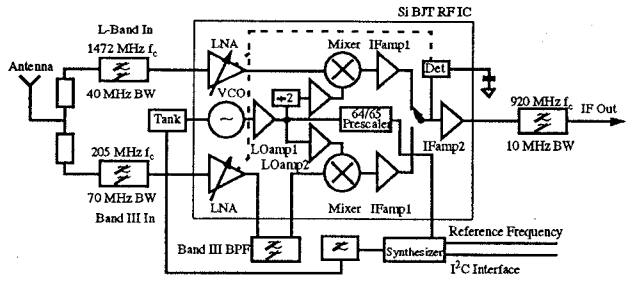

Figure 1 Si BJT dual band receiver RFIC

The L-Band and Band III chip inputs are directly connected to the DAB system antenna by respective fixed frequency filters configured as a diplexer with PCB board transmission lines. This input connection eliminates the rf loss, NF degradation and cost of a SPDT rf switch, but places additional isolation requirements on the RFIC which simultaneously sees both input Bands and must select between them.

Implemented in a 25 GHz f_T NPN bipolar process[4], the 88 x 88 mil IC is assembled into a fused lead plastic 28 pin SSOP package using 1 mil wire bonds. The common paddle ground with multiple chip-to-paddle down bonds and 4 fused ground leads are used to minimize ground inductance and conserve package leads. Figure 2 shows the IC in a cutout package with additional ground lead to paddle bonds to simulate the fused lead package during

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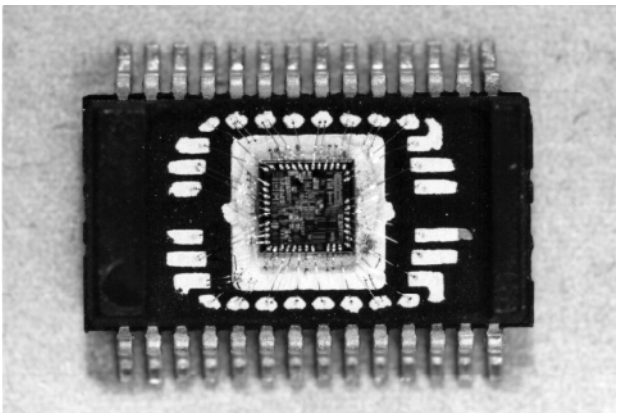

Figure 2 RFIC chip in a cutout SSOP-28 package

prototyping with negligible rf differences, but increased thermal resistance. Longer signal and Vcc bond wires, normally undesirable, resulting from down bonds to the paddle ground, are incorporated to enhance the L Band variable gain LNA operation and performance.

VARIABLE GAIN LNA DESIGNS

The variable gain LNAs are degenerated common emitter transconductance stages that use a current steering method to adjust between 20 dB maximum and –15 dB minimum gain. Single ended rather than differential designs are used to achieve minimum NF, provide direct connection to the diplexer and avoid costly external balanced to un-balanced converters (Baluns). Both LNA 50 Ohm ports have ESD protection circuitry, a commercial necessity that slightly degrades NF through substrate coupling. Both use either the diplexer or a low cost off-chip capacitor for input DC blocking to avoid additional NF degradation.

The L Band LNA 1st stage simplified schematic is shown in Figure 3.[1] A 2nd fixed gain stage follows providing additional gain at 1.5 GHz. Parallel connected NPNs in cascode "steer" rf signal between a load and a filter that isolates the signal from the LNA output, resulting in the variable gain. The filter is constructed from a careful arrangement of package leads and bond wires, seen in Figure 2 and on-chip components, overcoming the lack of a precise on-chip rf ground otherwise required for 30 dB isolation in a non-differential circuit.

For the –97 dBm sensitivity, a 2.5 dB LNA NF is required at maximum gain while at the high input power levels greater than 40 dB suppression of third order intermod-ulation products, IM3, is required. Planar inductors (Q = 3, 1.5GHz) and bond wires (Q = 60) are used for emitter degeneration, series feedback and reactive gain/noise matching. The higher Q of the package leads (Q=300) and

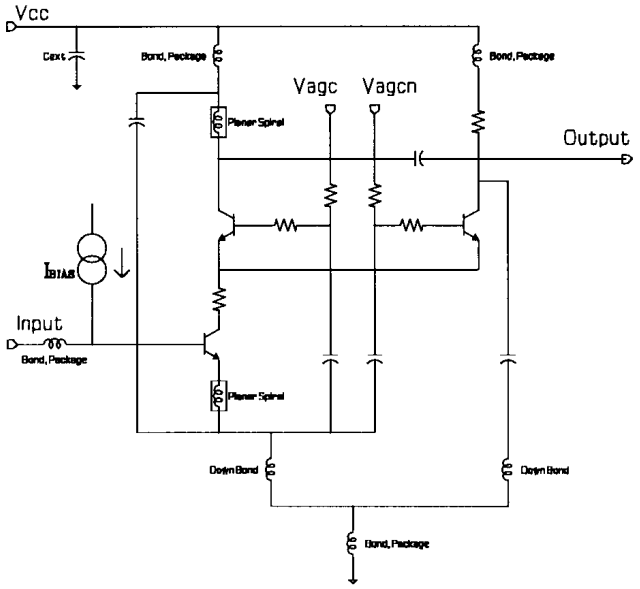

Figure 3 Simplified L Band LNA 1st stage schematic

bond wires helps to improve the otherwise low Q achieved from on-chip inductors alone. Five on-chip inductors are implemented in top level metal, 10um width, 2um spacing and vary in value from 1nH to 6nH. The combined package lead and bond inductance varies from 0.6nH to 4nH. Image frequency noise at 348 - 388 MHz is suppressed 12 dB by both reactive load matching and an on-chip LC filter/matching network before the mixer. An improved 25 dB image rejection is expected from adjustments to this filter in the next revision of the RFIC.

The Band III LNA simplified schematic is shown in Figure 4. In contrast to the reactively matched L Band

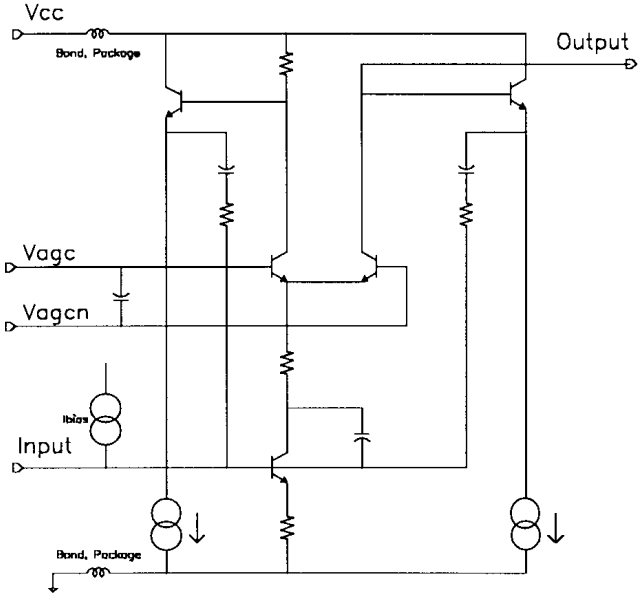

Figure 4 Simplified Band III LNA schematic

[1] Patent pending

design, parallel feedback through emitter followers is used to match the input impedance while gain is varied by the current steering method. The output is open collector and directly drives an off-chip filter/ impedance-transformer that provides a inductive path to VCC for maximum headroom. This 2 capacitor, 2 inductor filter provides 20 dB suppression of 2nd harmonic, and 40 dB suppression of 4th harmonic and works with the mixer RF/IF isolation to suppress spurious signals at the 920 MHz IF. Image noise at 2GHz is also well attenuated.

MIXER/IF DESIGN

Both mixers are a low current, high dynamic range modified Gilbert cell mixer design including an active class AB RF 180 degree splitter [5]. The 9mW DC design provides 55 to 60 dB IM3 suppression at the AGC leveled input power, near 0 dB conversion gain and 40 dB RF to IF isolation from its fully balanced topology. Used as a down-converter for L Band and as an up-converter for Band III, the MICROMIXER's relatively high 15 dB NF is shielded with the relatively high LNA gains permitted by the RFIC chip's variable gain architecture. The mixers also serve as single-ended to differential converters. The IF buffers are 2 parallel emitter degenerated differential input stages, combined at common resistor loads and followed by a shared, common emitter degenerated, open collector output stage that is used to maintain high linearity at IF output powers up to -10 dBm.

AGC/BAND SWITCH DESIGN

A single on-chip detector and AGC circuitry shown in Figure 5 are used to control both LNA gains by full wave rectification of the amplified, coupled IF signal then compared to a internally generated reference voltage by a transconductance stage. Between DAB signal frames, it can be desirable to freeze the AGC, which is done by extinguishing the charging current from the g_m stage.

All of the rf circuits on the IC use band gap references and PTAT bias circuits to maintain constant circuit gain over temperature. Power management logic shuts down individual references to turn off the amplifier and mixer portions of the chip and save 40 mA 5V DC power consumption. Switching between L Band and Band III paths is done by selectively powering down the amplifier and mixer portions of the unused path with a resulting isolation of greater than 60 dB for input powers up to 0 dBm.

VCO/PRESCALER DESIGN

The VCO, which is similar to the design shown in reference [6], employs a pair of cross coupled collector, differentially connected, bipolar transistors to realize a balanced oscillator coupled to an external LC tank. The tank inductance consists of a lead/bond inductance, and either a chip inductor or a printed microstrip line. Tuning capacitance, provided by a high-Q, abrupt junction varactor diode, minimizes phase noise achieving -90 dBc/Hz at 10 KHz offset for 130 MHz tuning range. The VCO is biased from a 3.3V regulator integrated on the IFIC [1].

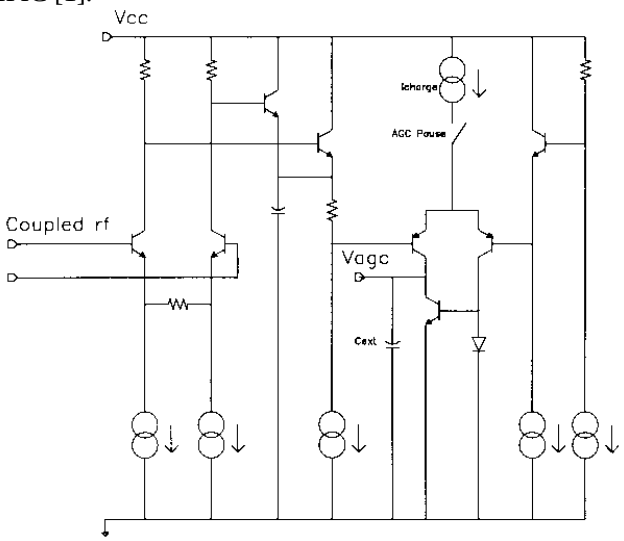

Figure 5 Simplified AGC schematic

The divide by 64/65 prescaler circuit is realized using 3 level balanced emitter coupled logic gates with CTAT biasing. A high speed divide by 2/3 using a pulse swallowing technique is followed by a series connected divide by 32 flipflop circuit. Separate prescaler 3.5V Vcc and ground package leads are used to minimize spurious leakage to other integrated analog circuits that could potentially degrade sensitivity. Measurement of the highest prescaler harmonic leakage to L Band input, the 85th, is -109 dBm, below the -97 dBm receiver sensitivity for a 8 dB C/N. For Band III, the highest prescaler harmonic leakage, the 12th is -98 dBm, a good result, but one which is nearly equal the weakest receive signal. Fortunately, the discreet multi-tone (DMT) modulation and digital forward error correction schemes employed by the DAB receiver make it insensitive to information lost from a single carrier or tone, a feature also important for its insensitivity to multipath propagation effects.

MEASURED PERFORMANCE

The L Band and Band III measured dynamic responses of the packaged IC are shown in Figures 6 and 7 respectively. It is seen that L Band IM3 remains above 40 dB up to input levels of -5 dBm and Band III IM3 remains above 50 dB up to input levels of -10 dBm. Both IM3 vary less than -0.05 dB/deg C from -40 to +115 deg C, improving with increasing temperature. Table 1 contains a summary of several thousand ICs measured at 25 degree C unless

Table 1

Measurement	Average Value	Standard Deviation
L Band Channel		
Conversion Gain	25.5 dB	0.4 dB
Variable Gain Range	30 dB	
NF (maximum gain)	4.7 dB	0.1 dB
IIP3 (-8 dBm input)	12.5 dBm	
Band III Channel		
Conversion Gain	27.5 dB	0.4 dB
Variable Gain Range	35 dB	
NF (maximum gain)	3.7 dB	0.2 dB
IIP3 (-13 dBm input)	14.5 dBm	
Full Chip		
Conv. Gain vs Temp. (-40 to +115 deg C)	< 0.01 dB/degC both channels	
NF vs Temp (-40 to +115 deg C)	< 0.01 dB/deg C both channels	
VCO phase noise at 10 KHz offset	-90 dBc/Hz	
Prescaler output	94 mVrms	
DC Power Consumption	330 mW	

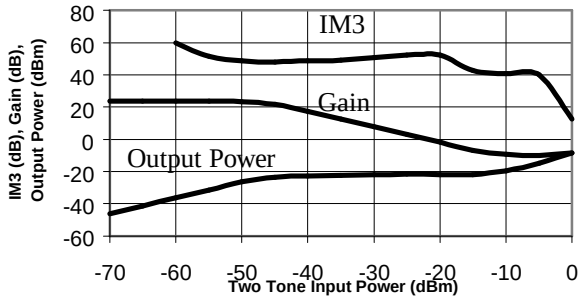

Figure 6 Measured 1.5 GHz L Band dynamic response

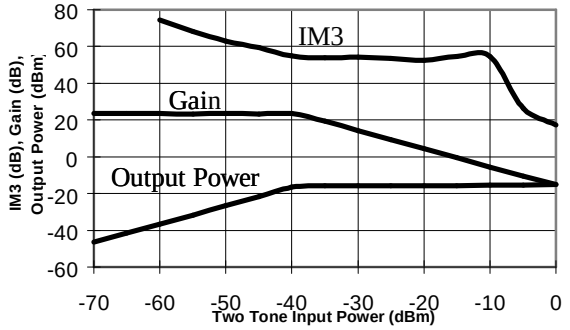

Figure 7 Measured 200 MHz Band III dynamic response

specified. A chip photo is shown in Figure 8. Over its 35 dB gain range, Band III LNA NF increases from 2.4 to 20 dB, considerably less than a dB increase for dB gain reduction. The L Band path performs similarly, insuring an increasing system C/N ratio with input power.

CONCLUSIONS

An RF IC has been presented which provides a dual channel down conversion and AGC function with exemplary dynamic range for a broadband system architecture which eliminates a preselection filter. The circuit is fabricated using a low cost Si bipolar process, and package, enabling the low cost manufacture of a DAB car radio receiver.

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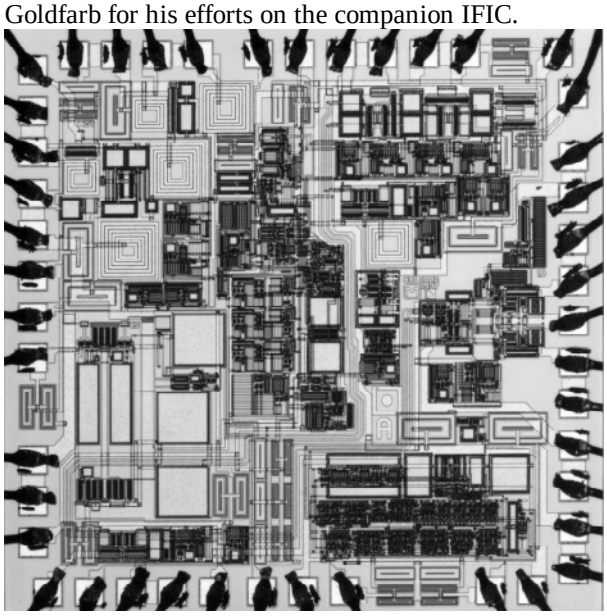

Figure 8 A photograph of the RFIC Chip

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